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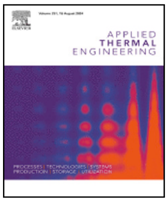

Research Paper

The impact of device architecture on the thermal response of AlN/AlGaN digital alloy field-effect transistors

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ABSTRACT

A digital alloy is a superlattice-like nanostructure formed by stacking ultra-thin (≤4 monolayers) AlN and GaN layers periodically. Digital alloys allow for the tunability of the bandgap and electrical transport behavior. However, for them to be explored for electronic device applications, it is crucial that we determine their thermal properties, as this greatly impacts the thermal resistance and heat spreading within a device. Here we investigate the thermal properties of various AlN/AlGaN and $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ digital alloys (where x and y are the associated alloy composition) are investigated using the combined techniques of time-domain thermoreflectance and steady-state thermoreflectance. A highly anisotropic thermal conductivity of 9.6 W/m-K (cross-plane) and 39.8 W/m-K (in-plane) was measured for an AlN/AlGaN digital alloy (0.86/5.93 nm period thickness), while all measured $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ digital alloys measured a thermal conductivity of 2.9–3.3 W/m-K (cross-plane) and 8.6 W/m-K (in-plane). To investigate the influence of these thermal properties have on in-planedevice thermal transport, a number of die-level thermal management approaches are investigated on an AlGaN metal–semiconductor field-effect transistor using numerical simulations. The effects of the various cooling approaches on the device channel temperature were comprehensively investigated, along with guidance for material selection to enable the most effective thermal solutions. Specifically, we investigate the influence of substrate material, top-side heat spreader thickness/thermal conductivity, digital alloy thickness, and flip-chip design. Overall, this numerical study shows that it is possible to achieve high power digital alloy device operation with appropriate die-level thermal management solutions.

1. Introduction

$Al_xGa_{1-x}N/Al_yGa_{1-y}N$ (where x and y are the associated alloy composition) short period superlattices (SPSL) provide a unique approach to tailor the bandgap and lattice constant of the resulting material by adjusting the thicknesses and the compositions of the individual layers of the superlattice unit cell. In past, AlN/AlGaN SPSLs were used to fabricate $Al_xGa_{1-x}N$ digital alloys with varying bandgaps [1,2]. Such digital alloys (DAs) have been used for strain management, and as the main light emitting layers for deep ultraviolet light emitting diodes (LEDs) and lasers [3–5]. Due to carrier confinement and energy level quantization, the emission energies of these digital alloy based LEDs can also be controlled by adjusting of the unit cell layer thicknesses.

In addition to utilizing the band-to-band transitions in the AlN/AlGaN digital alloys for optical devices, several groups have exploited the inter-sub-band transitions for optoelectronic devices in the infrared part of the spectrum [6]. Due to the strong spontaneous polarization in the AlGaN material system, the digital alloy superlattices can have extremely large charge densities accumulated at the interfaces. These charges can serve as a strong absorber in the IR part of the spectrum providing a basis for detectors.

In addition to the bandgap control, digital alloys also provide a unique approach to control doping and transport properties in the resulting DA-$Al_xGa_{1-x}N$ epitaxial layers. It was reported that co-doping in AlN/AlGaN digital alloys can potentially reduce the activation energy for p-type dopants such as Mg—thereby providing an approach leading to high p-type doping $Al_{0.83}Ga_{0.17}N$. Electrically, the alternating layers of different materials in digital alloys act as potential barriers that trap electrons within well-defined regions, resulting in discrete energy

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levels for the electrons (i.e., quantum wells). This quantum confinement effect leads to a reduction in the effective mass of the electrons, which significantly increases their mobility and conductivity. Additionally, the periodic structure of digital alloys allows for the creation of multiple parallel two-dimensional electron gases (2DEGs). The presence of multiple 2DEG channels can increase the current carrying capacity of the device and it reduces the sheet resistance of the material. These characteristics are ideal for improving the electrical performance of the high electron mobility transistors (HFETs) when such DA-$Al_xGa_{1-x}N$ layers are used for the device channel region.

Thermally, there are some critical differences between $Al_xGa_{1-x}N$ and digital alloys. Within $Al_xGa_{1-x}N$, random alloy scattering limits the mean free path of phonons, decreasing the thermal conductivity from their GaN (i.e., 253 W/m-K) and AlN (i.e., 321 W/m-K) counterparts to a range of 9–13 W/m-K for $x = 0.2$–0.8 [7]. For DA-AlN/AlGaN there is no random alloy scattering within the AlN layers. Instead, the mean free path of phonons is limited by scattering at the interfaces between adjacent layers of AlN and AlGaN. As such, these interfaces impede heat transport perpendicular to the interfaces (cross-plane direction) within the digital alloy, lowering the effective thermal conductivity of the AlN/AlGaN digital alloy significantly from that of AlN or GaN. For $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ digital alloys, both random alloy scattering and phonon-boundary scattering occurs. Interestingly, Zalewska et al. found $Al_xGa_{1-x}N$/AlGaN superlattices (x = 0.225–0.28) to have a highly anisotropic thermal conductivity (room temperature) of 5.1–10.3 W/m-K (cross-plane) and 19.7–32.9 W/m-K (in-plane) for period thickness of 4.8–44.6 nm [8]. Phonons in the $Al_xGa_{1-x}N$ layers were found to be predominantly limited by random alloy scattering, while phonons in the GaN layers were found to be limited by phonon-boundary scattering. Molecular dynamics simulations of superlattice structures in literature show evidence that, as period thickness decreases, complex scattering interactions between the layers that can lead to new phonon modes and coherent phonon modes across the layers [9]. As such, understanding or predicting the thermal conductivity of digital alloys is complex. An advantage of $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ digital alloys over AlN/AlGaN digital alloys is that it is much easier to find a common deposition condition for $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ than AlN and GaN. The growth of AlN and GaN layers requires precise control of deposition parameters, as their differing chemical bond stabilities lead to decomposition at different temperatures, complicating the simultaneous optimization of growth conditions [10]. As such, it is more practical to grow $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ digital alloys. The improved deposition conditions of $AlxGa1 - xN/AlyGa1 - yN$ digital alloys are expected to enhance crystallinity and layer uniformity, which could contribute to higher thermal conductivity. However, given the presence of significant random alloy scattering in these materials, phonon mean free paths are still likely to be strongly limited by alloy disorder, thereby constraining the overall thermal conductivity [7]. Given the recent push to develop digital alloy materials and the ongoing refinement of their deposition processes, a significant challenge for the research community in developing digital alloy HEMTs is the limited knowledge of their thermal properties. This lack of data hinders the ability to accurately explore and optimize thermal management strategies for future digital alloy HEMTs through thermal simulations.

In this paper, we experimentally measure the anisotropic thermal conductivity of various AlN/AlGaN and $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ digital alloy films using the TDTR and SSTR thermoreflectance techniques. The resulting thermal conductivity data is used as input into a 3D thermal model of a digital alloy HEMT device. We applied a heat flux near the drain-side of the gate to thermally simulate the device during operation and determine its maximum operating temperature and trends in thermal response. Additionally, we explored variations in the device architecture to promote improved heat dissipation at the die level. Ultimately, we found that the combination of multiple thermal management techniques resulted in the lowest operating temperature.

2. Methods

2.1. Experimental methods

In order to determine proper AlN/AlGaN and $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ digital alloy thermophysical properties to use in our thermal model, experiments were performed on AlN/AlGaN and $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ samples grown via Metal Modulated Epitaxy (MME) on Sapphire substrates. MME is a modified growth technique utilized in molecular beam epitaxy (MBE) where the group-III metal fluxes are periodically interrupted through the use of individual shutters while maintaining a constant active nitrogen supply [11–13]. Because the growth occurs under nominally metal rich conditions, cycling the metal fluxes leads to regimes of metal accumulation and metal consumption which can be tracked using reflective high energy electron diffraction (RHEED). Properly controlling the timings of these regimes prevents the formation of detrimental metallic droplets on the surface, removing the concern for droplet related defects. This is counter to traditional MBE growth which requires long term growth interrupts to prevent droplet related parasitic growth. Because the entire MME process is cyclical in nature, it can be an ideal growth method for realizing periodic structures. For the samples discussed in this paper, the MME growth process was altered slightly in order to achieve AlN/AlGaN superlattices. While the Al flux was modulated (using a 20 s open, 21.5 s closed timing), the supply of Ga was kept constant throughout the growth. This resulted in Ga acting as a surfactant during the growth of the AlN layers due to the preferential incorporation of Al over Ga. AlGaN layer formation then occurred during the portion of time when the Al bilayer was being consumed while GaN formation was prevented due to an 800 C substrate temperature.

Time-domain thermoreflectance (TDTR) and steady-state thermoreflectance (SSTR) measurements were performed to determine cross-plane thermal conductivity (k_z), in-plane thermal conductivity (k_r), and the thermal boundary conductance (TBC) of the metal transducer/digital alloy interface, by taking advantage of the complementary sensitivities of the two techniques. Prior to measurement, 86 nm of Aluminum was deposited onto the surface of the sample via electron beam evaporation at 1.2e–7 Torr. The thickness of the transducer was confirmed via picosecond acoustic measurements using the TDTR setup.

Within the TDTR and SSTR thermal models, the material properties of each layer for the fabricated samples are shown in Table 1. For the AlN/AlGaN DA, the heat capacity was assumed to be 2.66 MJ/m^3-K, a weighted average of the heat capacities of AlN and GaN, weighted by the layer composition and thickness of each material within a single period of the alloy (5.8 nm and 0.86 nm for AlN and GaN). The thickness of the digital alloy layers were measured using transmission electron microscopy, shown in Fig. 1.

Sensitivity analysis revealed that TDTR is over 20 times more sensitive to the cross-plane thermal conductivity of the digital alloy compared to the in-plane thermal conductivity (shown in supplemental). Conversely, sensitivity analysis (shown in supplemental) revealed that SSTR is sensitive to both cross-plane and in-plane thermal conductivities of the digital alloy layer. Additionally, sensitivity analysis revealed that we are completely insensitive to the TBR between the digital alloy and the AlN buffer below it, and was assumed to be 1 $m^2 - K/GW$. Setting the value of this TBR to 20 $m^2 - K/GW$ resulted in less than a 1% change in our fitted values for k_z and k_r.

To minimize the contour uncertainty of our measurements, we utilize a hybrid fitting technique, which allows us to fit both TDTR and SSTR datasets simultaneously [14]. In this hybrid fitting scheme, the thermal model and numerical fitting algorithm are tasked with determining a combination of three unknowns (i.e., $k_{z,DA}$, $k_{r,DA}$, and $TBR_{Al/DA}$) that yields an acceptable fit for both TDTR and SSTR datasets. The fitting process utilizes existing numerical tools, such as Python's scipy minimize function, where the residual is calculated independently for each dataset and model. The maximum residual, which

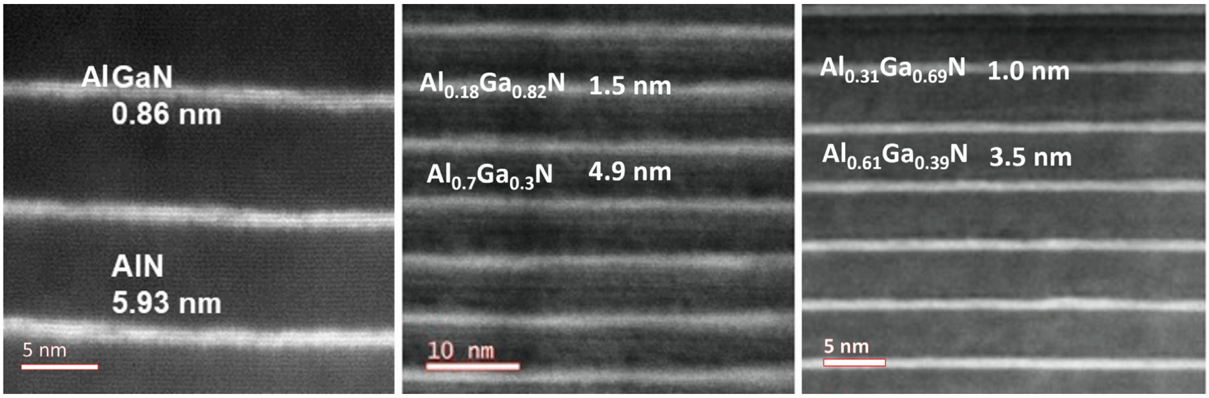

Fig. 1. Transmission electron-microscope image of the measured AlN/AlGaN and AlGaN/AlGaN digital alloys.

Table 1
Material properties for TDTR and SSTR analysis.

Layer	Material	Thickness (nm)	k (W m^{-1} K^{-1})	c_p (J kg^{-1} K^{-1})	ρ (g cm^{-3})
Film	Al	80.0 ± 2.0	189.0 ± 5.7	126.0 ± 3.0	19.3 ± 0.48
	AlN/AlGaN DA	1500 ± 50.0	Fitted	449.0 ± 11.1	7.19 ± 0.18
	AlN Buffer	434 ± 14.0	321 ± 10.2	451.0 ± 11.2	3.28 ± 0.08
Substrate	Al_2O_3	1.0×10^6	32.0 ± 3.2	710.0 ± 17.8	5.95 ± 0.14

represents the worst fit between SSTR and TDTR, is then passed to the minimization function to ensure that the worst-fitting dataset drives the overall fit. Additionally, we adopt the residual value approach (i.e., 1% residual), instead of using a mean squared error, to avoid potential issues associated with differently weighting datasets due to variations in data scaling or dataset lengths [14].

The cross-plane thermal conductivity of the AlN/AlGaN digital alloy was determined to be k_z = 9.6 ± 0.5 W/m-K. The in-plane thermal conductivity of the AlN/AlGaN digital alloy was determined to be k_r = 39.8 ± 2.1 W/m-K. We tabulate all thermal measurement values in Table 2. We hypothesize that the highly anisotropic thermal conductivity is a result of phonons having longer mean free paths while traveling in-plane in the digital alloy, compared to crossing multiple AlN/AlGaN interfaces. Meanwhile, our measurements of $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ digital alloys revealed a lower thermal conductivity (k_z = 2.9–3.5 W/m-K, k_r = 8.6 W/m-K). We suspect alloy scattering of the phonons to truncate the mean free path of phonons in the $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ digital alloys, limiting their thermal conductivity.

As demonstrated in Zalewska et al. the cross-plane thermal conductivity of AlGaN/GaN digital alloys, which are closely analogous in composition and structure to the AlGaN/AlN digital alloys studied in our work, remained nearly constant over a temperature range of 140 K to 340 K, despite a significant variation in the thickness of the period from 4.8 to 44.8 nm [8]. This suggests that phonon transport in these digital alloys is not primarily limited by boundary scattering but is instead dominated by alloy scattering within the AlGaN layers and interfacial scattering between the digital alloy layers. Tran et al. similarly found very little dependence on thermal conductivity of $Al_{0.5}Ga_{0.5}N$ films and film thicknesses, with thermal conductivity varying from 7.5–8.8 W/m-K for films from 1–10 μm thick [7].

Given the close structural and compositional similarity between AlGaN/GaN and AlGaN/AlN digital alloys, these findings provide reasonable experimental support for our assumption of relatively constant thermal conductivity in the digital alloy layer with changing temperature (see Table 2).

2.2. Simulation methods

Having determined the thermal conductivity of several digital alloys, our goal was to determine the resulting impact of thermal conductivity on the thermal trends of real HEMT devices. To do so, 3D finite element models were constructed based on the AlN/AlGaN HEMT layout [Fig. 2] and the various cooling structures shown in Fig. 3. The temperature-independent thermal conductivity and thermal boundary conductance values used for each material layer and interface are summarized in Table 3. While it is well established that thermal conductivity and interfacial thermal resistance can exhibit temperature dependence, comprehensive experimental data for these dependencies are not available for many of the materials and interfaces relevant to our study. Consequently, we employ room-temperature values for thermal conductivity and thermal boundary resistance, ensuring consistency and enabling a clear evaluation of how different thermal management strategies influence the temperature rise in digital alloy HEMT devices. Despite this simplification, our approach remains highly valuable, as it allows for a systematic comparison of design parameters and provides key insights into the relative effectiveness of various cooling techniques when applied to emerging digital alloy-based HEMT architectures. For our heat generation source, a thermal dissipated power density of 2 W/mm was applied to the top of the AlN/AlGaN DA, with half the heat flux applied underneath the gate, and the other half directly adjacent to the gate (on the drain-side), shown by the red box in Fig. 2. The location and dimension of the heat source was assumed to be independent of bias condition or power density. A progressive tetrahedral mesh was generated to discretize the domain with the finest and highest density mesh elements in the region close to heat generation volume. The density of mesh elements was decreased gradually upon moving down through the material stack. For layout A, B, C and D models shown in Fig. 3, the mesh consists of approximately 500 000, 800 000, 400 000, and 1 500 000 elements, respectively. The final model is solved by the steady-state finite element analysis in ANSYS. Mesh convergence testing was carried out for all of the results reported in the study, and the results were found to be mesh-independent.

For each layout, we investigate the effect of various parameters of the device architecture on maximum channel temperature (T_{max}) by varying the components' parameters within a feasible range. We also chose a set of parametric conditions to form the baseline model with these values being conservative estimates of what is expected for nominal devices. The heat sink was treated to be a 25 °C isothermal boundary condition, and a natural convection heat transfer coefficient (HTC) of 10 W/m^2-K was applied at the device surface exposed to the ambient to represent natural convection. The environment temperature

Table 2
Summary of thermal properties of AlGaN/AlGaN and AlN/AlGaN digital alloys measured experimentally.

Material 1	Material 2	Material 1 (nm)	Material 2 (nm)	Film (μm)	k_z (W m^{-1} K^{-1})	k_r (W m^{-1} K^{-1})
AlGaN (8% Al)	AlGaN (65% Al)	2.1	7.0	0.4	3.3	–
AlGaN (31% Al)	AlGaN (61% Al)	1.0	3.5	0.4	2.9	–
AlGaN (40% Al)	AlGaN (70% Al)	4.0	5.0	0.4	3.5	–
AlGaN (18% Al)	AlGaN (70% Al)	1.5	4.9	0.4	3.1	–
AlGaN (18% Al)	AlGaN (70% Al)	1.5	4.9	5.0	3.0	8.6
AlGaN (90% Al)	AlN	0.86	5.93	1.5	9.6	39.8

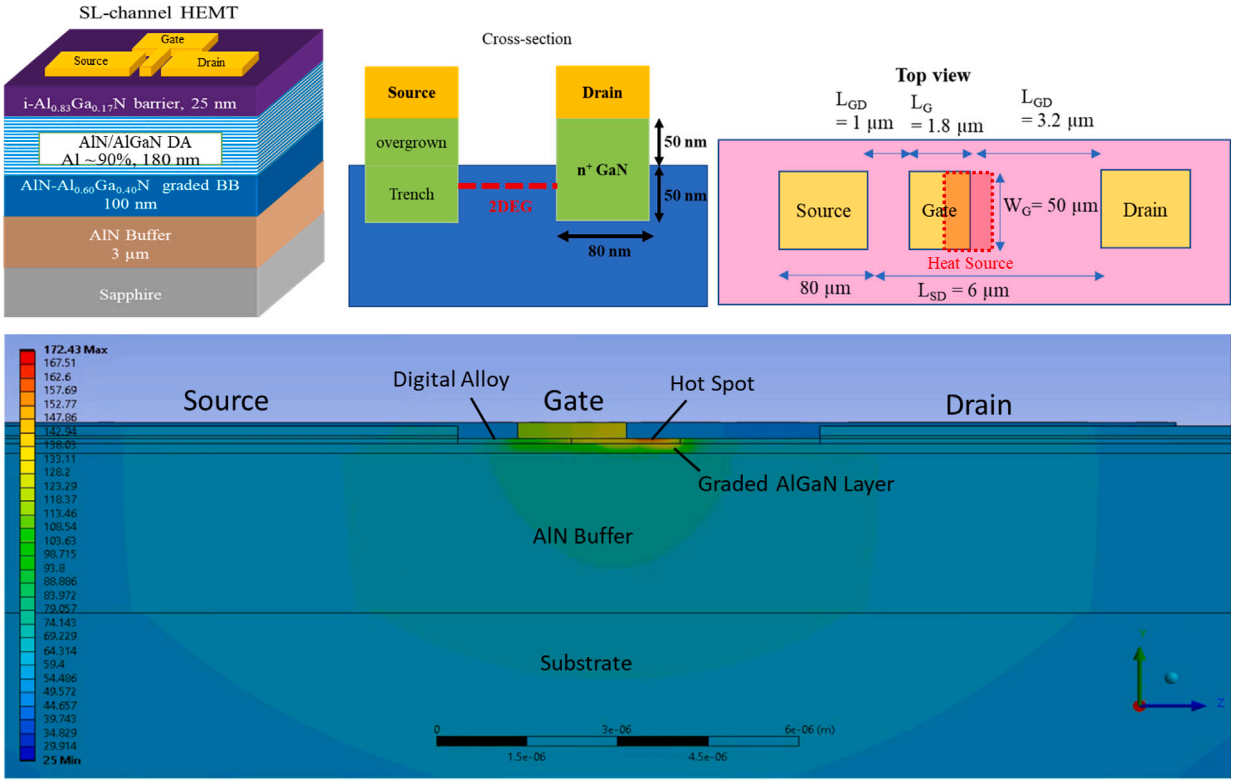

Fig. 2. Schematic layout of the investigated single-fingered AlN/AlGaN digital alloy field-effect transistor. Also shown, is a temperature contour of our simulation, showing the hot spot located near the drain-side of the gate.

was assumed to be 25 °C. For graded AlGaN to AlN or AlGaN-DA interfaces, we assumed a TBR of 0.1 m^2-K GW^{-1} as the graded AlGaN composition was intentionally grown to be identical to the composition of AlN or AlGaN-DA directly at this interface, yielding a small TBR in practice due to the seamless interface. For GaN-based interfaces, we chose to use larger TBR values in our simulations to explore a worst-case scenario, ensuring our analysis accounts for potential thermal bottlenecks under less ideal conditions. We acknowledge that lower TBR values for GaN interfaces are reported in the literature, some reaching as low as 3–4 m^2-K GW^{-1} [15].

3. Results

3.1. Simulation results

For the original device, the maximum junction temperature (T_{max}) was evaluated for semiconductors in the active channel comprised of AlGaN, AlN/AlGaN digital alloy, and GaN. It should be noted that only the material properties of the semiconductor layer were altered for each iteration, not the entire device structure itself. As seen in Fig. 4a, The low thermal conductivity of AlGaN (9 W/m-K) and AlN/AlGaN DAs (9.6 W/m-K, 39.8 W/m-K) results in heat from joule heating to accumulate in the semiconductor layer, leading to large T_{max} in the original device compared to that of GaN. Switching from an AlGaN

Table 3
Summary of thermal properties used in the 3D finite element models of the various cooling structures.

Material	Thermal conductivity (W m^{-1} K^{-1})
AlGaN	9.0 [16]
AlN/AlGaN DA	9.6 (k_z) 39.8 (k_r)
GaN	253.0 [17]
Al$_2$O$_3$	32.0
AlN	310.0 [18]
SiC	490.0 [19]
Interface	Thermal boundary resistance (m^2-K GW^{-1})
AlN/AlGaN-DA/Heat Spreader	10.0 [20]
AlN/AlGaN-DA/Metal	9.2 (Measured for Al/AlN/AlGaN-DA)
AlN/AlGaN-DA/Graded AlGaN	0.1 (Assumed)
Graded AlGaN/Al$_2$O$_3$	8.0 [21]
Graded AlGaN/AlN	0.1 (Assumed)
Graded AlGaN/SiC	6.3 [22]
GaN/Al$_2$O$_3$	67.0 [23]
GaN/SiC	10.1 [22]
GaN/AlN	47.6 [21]

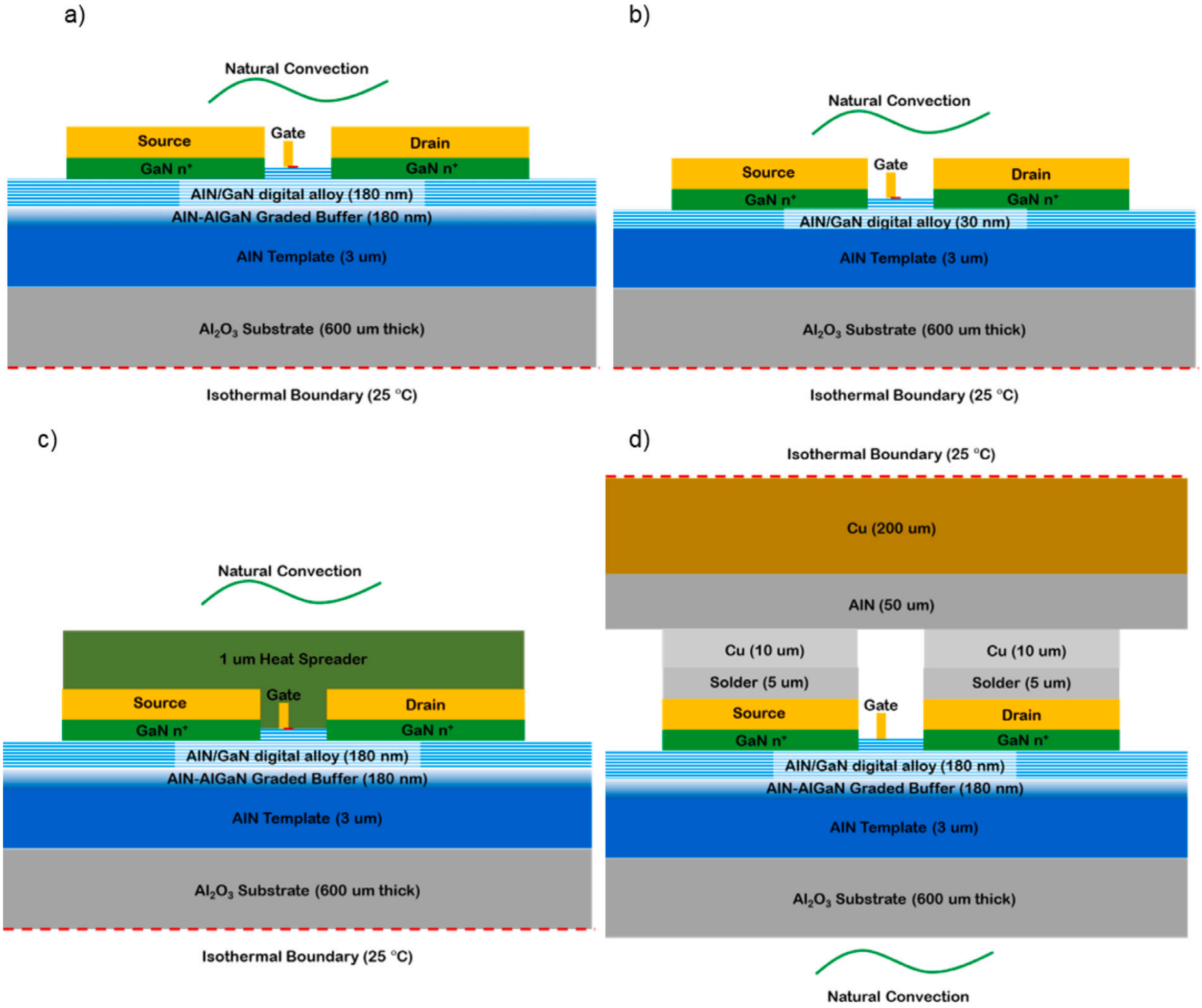

Fig. 3. Schematic of each device layout tested for the single-fingered AlN/AlGaN digital alloy field-effect transistor. (a) The original device structure. (b) Removal of the graded AlGaN layer and thinning of the AlN/AlGaN digital alloy layer. (c) The inclusion of a top-side heat spreader. (d) Flip-chip design of the device.

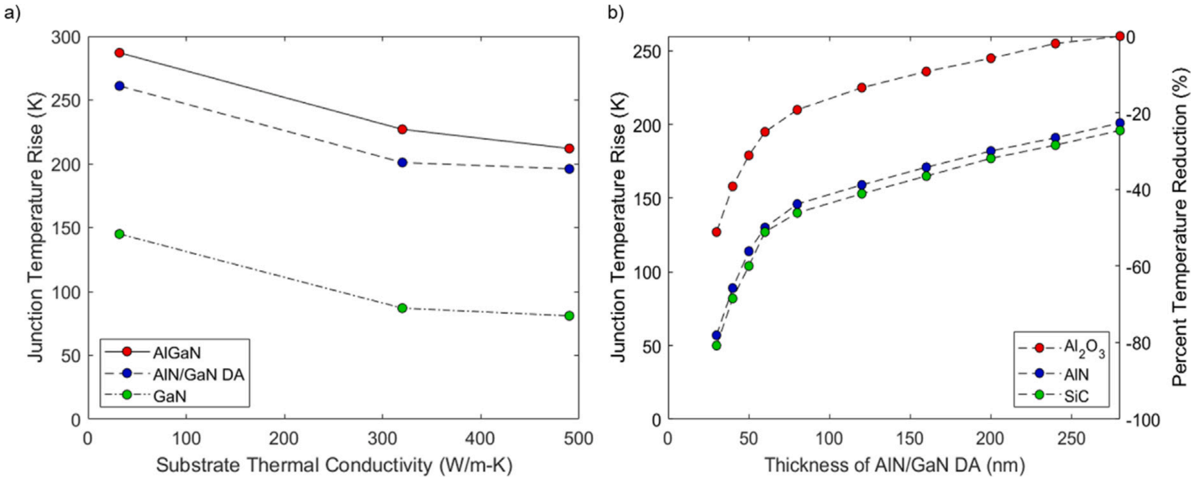

Fig. 4. (a) Graph of maximum junction temperature (T_{max}) as a function of substrate thermal conductivity for varying materials for the semiconducting layer. (b) Graph of maximum junction temperature (T_{max}) as a function of digital alloy thickness for varying substrate materials.

semiconductor to a AlN/AlGaN digital alloy resulted in an reduction in T_{max}, as large as 10%. In this instance, the higher in-plane thermal conductivity of the AlN/AlGaN digital alloy (39.8 W/m-K) compared to AlGaN (9.6 W/m-K) assists in the lateral heat spreading, lowering T_{max} for the device compared to the AlGaN case. That said, the GaN semiconductor case still yielded a T_{max} 44% lower than that of the AlN/AlGaN digital alloy, due to GaN higher thermal conductivity (253 W/m-K). This shows that for AlN/AlGaN digital alloy devices to become a competitor of GaN devices, thermal management techniques must be considered to combat the temperature rise within digital alloy devices.

The first set of thermal management techniques inspected were bottom-side heat removal strategies, like the use of high thermal conductivity substrates and thinning the semiconductor layer to reduce thermal resistance and improve thermal response. Seen in Fig. 4a, changing from an Al_2O_3 substrate to either an AlN or SiC substrate significantly lowers T_{max} for both AlGaN (27% and 35% reduction) and AlN/AlGaN digital alloy (21% and 25% reduction). The use of high thermal conductivity substrates for bottom-side heat removal thus proves to be an effective strategy for lowering operating temperatures in AlN/AlGaN digital alloy devices. Additionally, for AlN or SiC substrate cases, the difference in T_{max} between AlGaN and AlN/AlGaN digital alloy is less significant (10% and 5.5% for AlN and SiC substrates) than for Al_2O_3 substrate. Notably, even with the higher thermal conductivity substrates, T_{max} of the AlN/AlGaN digital alloy devices still are larger than GaN devices with Al_2O_3 substrate.

A second bottom-side thermal management technique inspected is thinning of the AlN/AlGaN digital alloy. Since the GaN layers of a AlN/AlGaN digital alloy are so thin, they will naturally strain to match the lattice constant of the adjacent AlN films. As such, the use of a graded AlGaN layer may not be necessary to ensure crystalline digital alloy films. To test the influence of semiconductor thickness on T_{max}, we altered the combined thickness of the AlGaN graded film and the AlN/AlGaN digital alloy. This was done by removing material from the graded layer until it was depleted, then removing from the digital alloy layer. The resulting T_{max} for varying semiconductor thickness is shown in Fig. 4b, with T_{max} decreasing with semiconductor thickness. Notably, T_{max} reduction is roughly linear from 75–280 nm. However, between 30–75 nm, T_{max} reduction seems to increase rapidly with decreasing semiconductor thickness. We hypothesize that most of the lateral spreading of the heat occurs within the first 30–75 nm of the digital alloy, while most of the heat transfer in the 75–280 nm of the semiconductor is likely vertical. This would explain why T_{max} reduction is linear between 75–280 nm, since removing material would alter the effective thermal resistance according to linear conduction $R_{cond} = \frac{L}{K}$, where L is layer thickness and K is thermal conductivity. More notably, we find thinning of the semiconductor to dramatically lower T_{max} for the device, with a change from 280 nm to 30 nm thickness resulting in nearly a 51% reduction in T_{max}. We hypothesize the thermal conductivity of the AlN/AlGaN digital alloy to be constant across the thickness ranges tested, as the main limitation to phonon mean free path in the digital alloy is interfacial phonon scattering. As such, we do not expect much of the cross-plane thermal conductivity to come from long mean free path phonons, as most will be scattered at the interfaces of the digital alloy. Combining both bottom-side heat removal techniques, Using a high thermal conductivity substrate like AlN or SiC, and thinning the digital alloy, we find that nearly 79% reduction in T_{max} can be achieved. While the thermal conductivity of AlN (310 W/m-K) is lower than SiC (490 W/m-K), there seems to be negligible difference in T_{max} for the thinned digital alloy.

Top-side thermal management techniques were also investigated, specifically in the form of a heat spreader grown on-top of the original device (i.e., AlN/AlGaN semiconductor, Al_2O_3 substrate). The goal of top-side heat spreaders is to provide an alternative avenue for lateral heat spreading directly adjacent to the hot-spot in the junction, lowering T_{max}. Shown in Fig. 5a, a large range of heat spreader thermal conductivities and thicknesses were tested to find their associated T_{max}. The TBC between the device and the heat spreader was assumed to be 100 MW/m^2-K. For all cases, we find that a top-side heat spreader is capable of significantly reducing T_{max} for the device (i.e., 21%–51% reduction). Interestingly, we find that T_{max} depends more on the thickness of the heat spreader than the thermal conductivity of the heat spreader. For example, thin high-quality heat spreaders (i.e., 0.5-μm, 250 W/m-K) results in a similar T_{max} (186 K) as thicker low-quality heat spreaders (i.e., 3-μm, 50 W/m-K) (187 K).

In terms of application, thicker low-quality heat spreaders may offer more practical solutions than thin high-quality ones. For example, Anaya et al. measured the lateral thermal conductivity of a 1960 nm diamond film to be 85 W/m-K (first 490 nm), 175 W/m-K (second 490 nm), and 309 W/m-K (third 980 nm), with variations depending on the film's nucleation and growth regions [24]. While CVD-grown diamond has higher thermal conductivity, its cost and deposition complexities make it less practical for large-scale applications. In contrast, sputtered AlN, despite its lower thermal conductivity (ranging from 17–130 W/m-K for thicknesses between 150–3500 nm), offers significant cost advantages and is easier to deposit in large quantities [25]. Both polycrystalline diamond and AlN exhibit anisotropic thermal conductivity influenced by grain size and defects. Diamond and AlN typically show lower in-plane (lateral) conductivity due to grain boundary scattering, with higher cross-plane conductivity, particularly in films with larger grains [26,27]. Smaller grains lead to more isotropic but lower conductivity, as phonon scattering at grain boundaries increases. Larger grains enhance cross-plane thermal conductivity by reducing scattering along the grain growth direction [28,29]. However, the in-plane thermal conductivity does not vary much with film thickness, limiting improvement in lateral heat removal. Defects such as dislocations and impurities further decrease thermal conductivity in both materials by introducing additional phonon scattering centers [29]. Therefore, optimizing grain size and minimizing defects are essential for maximizing the thermal conductivity of both polycrystalline diamond and AlN heat spreaders.

One limitation of top-side heat spreaders is that they often exhibit poor TBC with the device materials [20,30]. To test the influence of TBC on T_{max}, we inspected the AlN/AlGaN device with 1 μm heat spreader on-top and altered the TBC between the device and the heat spreader. Shown in Fig. 5b, we find that T_{max} is more sensitive to heat spreader thermal conductivity than it is to device/heat spreader TBC. Even for low TBC values (i.e., 50 MW/m^2-K), a 250 W/m-K heat spreader was able to reduce T_{max} by nearly 39%. We find lower thermal conductivity heat spreaders to be even less sensitive to TBC, since a majority of the thermal resistance for lateral heat spreading comes from the lower thermal conductivity of the heat spreader. Others have shown an effective method for drastically improving the TBC of Diamond/AlGaN interfaces is the inclusion of a < 1 nm Si_3N_4 film at the interface [31]. These interfacial layers act as barriers to plasma which can etch at the GaN surface during diamond growth.

Lastly, we compare the effectiveness of all thermal management technique mentioned, as shown in Fig. 6. For comparison the original device is an AlN/AlGaN device, with an Al_2O_3 substrate, no heat spreader, and 280 nm of semiconducting material (as shown by the green bars in Fig. 6). We found that switching to higher thermal conductivity substrates, though reduced T_{max} by 23% and 31% for AlN and SiC, it was not enough to lower T_{max} below that of the GaN device. In comparison, adding a 1 μm thick top-side heat spreader resulted in similar reduction of T_{max} to the high thermal conductivity substrate, reaching a maximum of 36% reduction in T_{max}. Lastly, thinning the semiconductor films exhibited the largest reduction of T_{max}, with 51% reduction for removing the graded AlGaN layer and thinning the digital alloy layer to 30 nm. Notably, thinning alone was capable of lowering T_{max} below the T_{max} of the GaN device. Combining top-side and bottom-side techniques, we find adding a SiC substrate and a 250 W/m-K top-side heat spreader results in a 50% reduction of T_{max}, causing the device to have a T_{max} below that of the GaN device and retaining the graded AlGaN layer to assist the relaxation of the digital alloy film. Alternatively, the flip-chip design displayed a nearly identical T_{max} reduction without the use of expensive substrates or films grown on-top. Lastly, by combining each technique mentioned, we achieved the lowest T_{max} for this device in our simulations, with a 76% reduction in T_{max}. Though, it should also be noted that this is likely the most expensive solution.

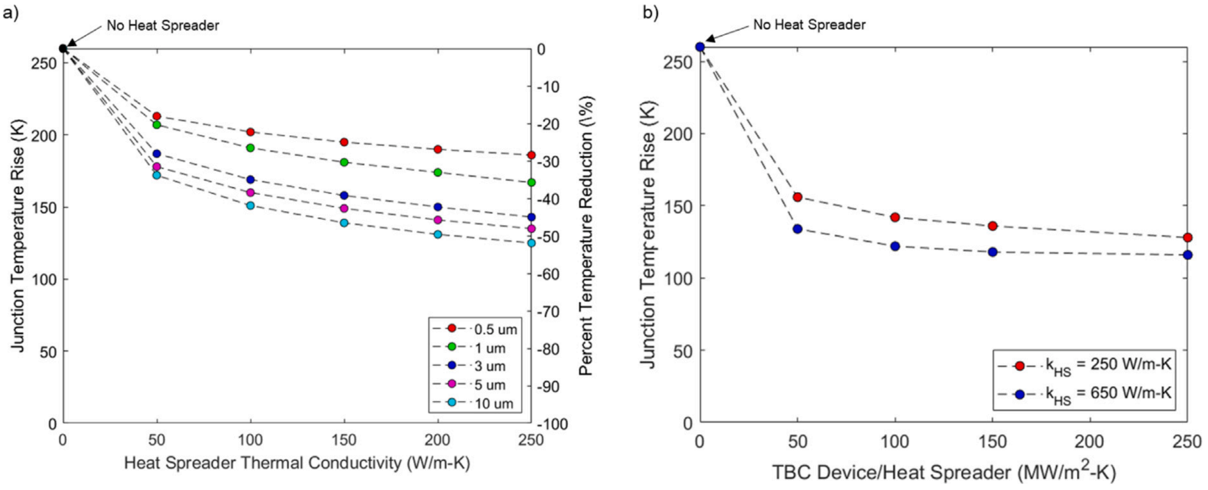

Fig. 5. (a) Graph of maximum junction temperature (T_{max}) as a function of heat spreader thermal conductivity for varying heat spreader thickness. (b) Graph of maximum junction temperature (T_{max}) as a function of device/heat spreader TBC for varying thermal conductivity heat spreader.

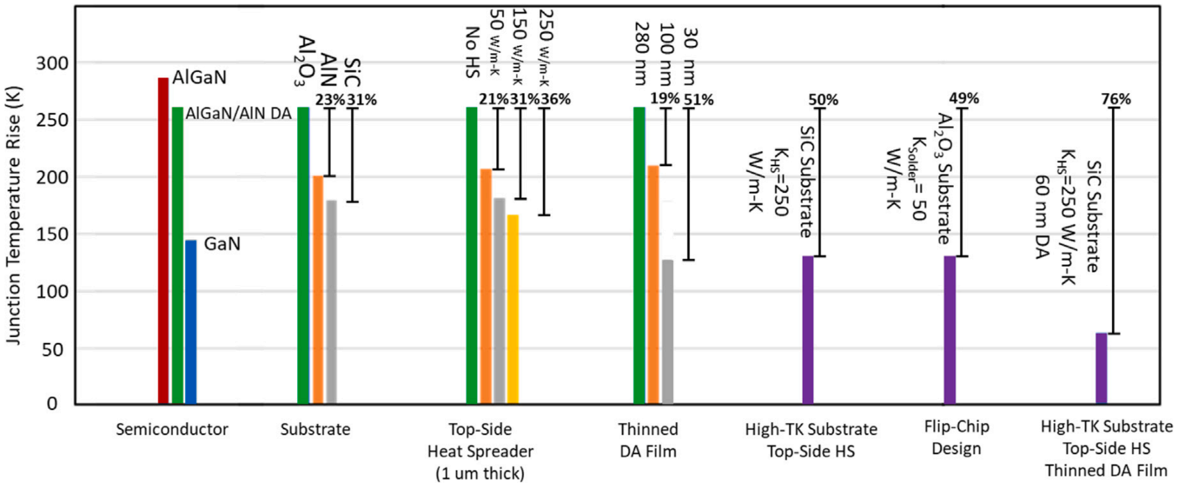

Fig. 6. Graph of maximum junction temperature (T_{max}) in comparison to each of the thermal management techniques discussed.

4. Conclusion

AlN/AlGaN and AlGaN/AlGaN digital alloys will present a challenge to device thermal management due to its inherently low and anisotropic thermal conductivity. However, several steps can be taken at the die level to help spread and manage the heat that is being dissipated, allowing for high power operation. For bottom-side cooling, high thermal conductivity substrates like AlN and SiC can reduce T_{max} by 23%–31%. For top-side cooling, 1 μm heat spreaders deposited on-top of the device were found to reduce T_{max} by 21%–36% for thermal conductivities ranging from 50–250 W/m-K. Lastly, thinning the graded AlGaN layer and the AlN/AlGaN digital alloy was found to be the most effective cooling method, reducing T_{max} by 51% when the film was reduced from 280 nm to 30 nm, making its T_{max} comparable to that of if GaN had been used. A double side cooling scheme utilizes both upper and lower thermal paths to extract the heat. Thus, the thermal dissipation ability is better than bottom side cooling and top side cooling alone. Combining all techniques, we found that T_{max} could be reduced by 76%, demonstrating the strength of combined thermal management techniques. Notably, this reduction is less than half the temperature rise observed for the GaN-based device, shown in blue in Fig. 6. As more is discovered about the electrical properties of AlN/AlGaN digital alloys, the thermal challenges presented by their low thermal conductivity will need to be combated with die-level thermal management techniques.

Code access

For full access to the fitting procedure and associated code used in this study, please refer to our GitHub repository: ExSiTE-Lab, TDTR Fitting Functions, GitHub, github.com/ExSiTE-Lab/TDTR_fitting

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary material related to this article can be found online at https://doi.org/10.1016/j.applthermaleng.2025.126677.

Data availability

Data will be made available on request.

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