Suspended Silicon Nitride Platforms for Thermal Sensing Applications in the Limit of Minimized Membrane Thickness

Ethan A. Scott, Hwijong Lee, John N. Nogan, Don Bethke, Peter A. Sharma, Patrick E. Hopkins, Tzu-Ming Lu, and C. Thomas Harris

***Abstract*— Silicon nitride has long been employed in the microfabrication of thermal sensors due to its favorable material properties and the ease with which it facilitates surface micromachining. While a variety of studies have utilized thin silicon nitride membranes for high sensitivity thermal measurements, limited reports exist on the physical characteristics of membranes and platforms in a thickness limit much less than 100 nm. Herein, we report on the development of low-stress, suspended silicon nitride platform devices that enable thermal characterization of membranes ranging from 120 nm to less than 10 nm in thickness, providing thermal conductivities as low as 1.1 W m^{-1} K^{-1} near room temperature. Applications of these platforms may enable appreciable enhancement in the performance of devices reliant upon environmental thermal isolation including bolometers, calorimeters, and gas sensors, among others. [2024-0003]**

***Index Terms*— Silicon nitride, membranes, thermal engineering, thermal sensors, thermal conductivity.**

I. Introduction

SILICON nitride (SiN) membranes are used in a number of applications including transmission electron microscopy [1], gas detectors [2], and microelectromechanical systems (MEMS) [3], [4], [5]. Often, SiN membranes are employed to provide isolation for thermal sensors or for studies requiring thermal isolation from a substrate [6]. Highly suspended structures may also be fabricated from such membranes, which further reduces the thermal conductance of the system [7], [8]. As the thermal conductance is inversely proportional to the length of the conducting medium, longer membrane tethers enable greater isolation. For example, Thompson et al. [9], have demonstrated SiN thermal platforms, several hundred nanometers thick with tethers several hundred microns in length.

Despite the ability to engineer ultra-low thermal conductance systems with long platform tethers, in some instances, device density requirements impose a practical length limitation. For example, most modern commercial bolometers employ detectors with individual sensors that fit within a sub-50 μm envelope [10], [11], [12]. This necessitates alternative approaches for reducing the thermal conductance, such as minimization of tether cross-sectional area by means of reducing thickness, width, or thermal conductivity of the tether.

The correlation between reduced membrane thickness and improved thermal isolation is straightforward. However, implementation of ultrathin (i.e., $\ll$ 100 nm) suspended devices, is challenging due to the potential for membrane failure during fabrication. Furthermore, accurate characterization of the thermal properties is particularly difficult, and thus, there are comparatively fewer works which have focused upon the thermal properties of suspended platforms in this ultrathin regime. For example, the intrinsically low thermal conductivity of SiN would result in low sensitivity to in-plane heat spreading within the membrane for thermoreflectectance-based techniques [13]. Electrothermal methods may alternatively be applied, which require special consideration for potential radiative effects on the measurement [14].

In this study, we discuss the development and thermal measurement of microfabricated, nanomembrane SiN devices with thicknesses nominally ranging from 120 nm to less than 10 nm. Thermal conductivity and thermal conductance measurements are reported for a range spanning 10 K to 300 K. Depending upon the membrane thickness, we observe thermal conductivities ranging from 1.1 W m^{-1} K^{-1} to 2.4 W m^{-1} K^{-1} near room temperature. The development of platforms in this ultrathin regime provides a path toward achieving devices with exceptionally low thermal conductances within an envelope applicable to commercial applications.

II. Experimental

A. Suspended Platform Development

A critical parameter for membrane structures is the intrinsic film stress. In cases where the film stress is compressive, wrinkling or deformation can occur [15], which is undesirable

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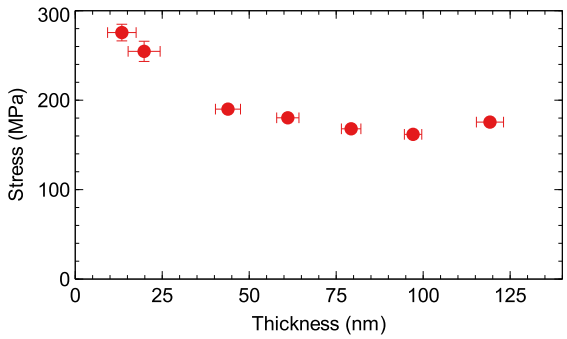

Fig. 1. Tensile film stress of SiN measured as a function of film thickness. The error bars display the standard deviation from multiple thickness and stress measurements performed during each round of etching.

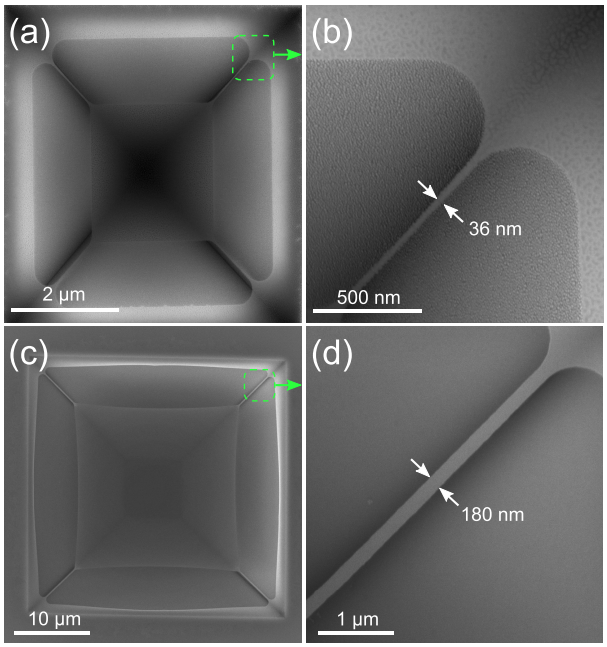

Fig. 2. Example SEM images of suspended platforms. Both platforms are nominally 18 nm thick. (a) and (c) display platforms with side lengths of 20 μm and 2.2 μm respectively. (b) and (d) show magnified images of the corresponding regions outlined in (a) and (c).

for device fabrication. In the other extreme, high tensile stress may lead to cracking or failure during membrane release processes [16] (although, highly tensile membranes ($\geq$ 1 GPa) are of interest for mechanical resonator applications [17], [18]). In general, however, films with low or moderately tensile intrinsic stress are preferable to ensure a flat surface with minimized potential for failure upon release.

Stress relief structures and tuning of the deposition recipe are among the most prevalent approaches to tailoring stress within thin membranes. For example, Shchepetov et al. [19] and others [20], [21], [22] have utilized stress compensation frames to mitigate compressive stress and eliminate wrinkling in thin silicon membranes. Alternatively, deposition parameters may be adjusted to alter intrinsic stress properties of thin film membranes. Habermehl [23], for example, has shown that the intrinsic stress of low pressure chemical vapor deposited (LPCVD) SiN is functionally dependent upon the Si volume fraction. Generally, films which are slightly silicon-rich compared to stoichiometric Si_3N_4 films provide a lower tensile stress.

We employ the latter approach and develop films with low tensile stress through control of the deposition parameters. We deposit films on (100) Si substrates by LPCVD at 840 °C in a Tystar Titan 4600 diffusion furnace using a mixture of NH_3 and H_2SiCl_2 (DCS). Following deposition, we characterize the film stress with a KLA-Tencore F2320 wafer bow measurement system. The curvature of the wafer and film is compared to that of a baseline curvature measurement taken prior to the deposition. This curvature is analyzed and related to the film stress through Stoney's Equation. We then etch the film with a reactive ion etch (RIE) process and repeat the stress measurement to observe the thickness-dependence of the film stress. Thickness measurements are performed via spectroscopic reflectometry (Nanometric Nanspec/AFT 210).

Fig 1 displays an example of the film stress for the SiN recipe used to develop the devices used in this study. For films with a thickness above 50 nm, the stress is tensile and relatively constant between 150 MPa - 200 MPa. As the film is etched to lower thicknesses, the tensile stress increases and approaches 280 MPa for films nominally 10 nm thick. Tensile stresses of several hundred MPa are not uncommon in SiN membrane structures [24], [25]. However, as SiN film stress is sensitive to deposition parameters including gas flow ratios and temperature, films with tensile stresses of lower magnitude are achievable as well as compressively stressed films [26], [27], [28], [29]. In the other extreme, certain applications such as mechanical resonators require membranes of high tensile stress,and suspended SiN structures with stresses in the range of GPa have been demonstrated, for example, in [17] and [18].

The relation between film stress and thickness shown in Fig. 1 can be explained by the gas flow sequence of the deposition. In short, separate deposition conditions are used in the early and later deposition stages. The early stage process is tuned to enable initiation of the CVD process and involves a DCS:NH_3 ratio of 3.5:1. Once the deposition is initiated, the DCS ratio is sequentially ramped to a value of 4.4:1, which is used for the main phase of the deposition. Full details of the process sequence are provided in the supplementary material. We find the relatively low level of tensile stress in these films to be suitable for the production of ultrathin, highly suspend structures. Fig. 2 demonstrates examples of suspended membranes fabricated from nominally 18 nm thick films. We utilize a top-down etch method (see section III) in which the silicon membrane is released by undercutting the substrate by anisotropic etching. This approach results in lower etch times compared to a backside etch process and is favorable for the fabrication of smaller device features. For example, large suspended platforms ($\geq$ 20 μm) may be produced with tethers on the order of 100 nm - 200 nm (Fig. 2(c,d)), as well as smaller platforms on the order of a few μm that have tethers only tens of nanometers wide (Fig. 2(a,d)). This flexibility of fabrication allows for the development of devices which can be tailored for characterization of thermal properties.

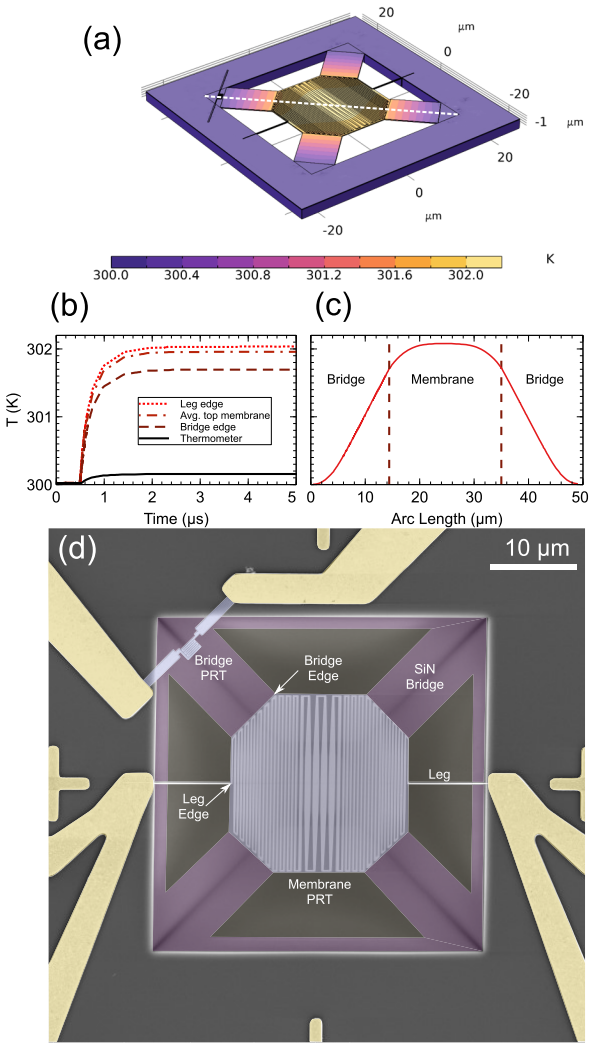

Fig. 3. (a) Example COMSOL model of the spatial temperature profile of a 120 nm thick membrane in response to a DC current bias of 2.5 μA. (b) displays the time-dependent temperature rise at various locations on the device. (c) displays the temperature profile along the dashed line in (a) 3 μs after the applied bias. (d) displays a colorized SEM micrograph of the nominally 20 nm thick device.

B. Thermal Device Design

For platform thermal measurements (specifically, the thermal conductivity of the silicon nitride and the overall thermal conductance of the system), we design devices with thin film resistance heaters and thermometers (i.e., platinum resistive thermometers (PRTs)) patterned upon the suspended silicon nitride. A schematic of the device design is shown in Fig. 3(a). The devices feature an octagonal membrane with a large, lithographically patterned PRT to serve as a combination heater-thermometer. There are four, wide, suspended SiN films that connect the membrane to the substrate. We refer to each individual suspended film as a bridge. At the edge of one bridge, we pattern another serpentine PRT to analyze the temperature drop along the length of the bridge. Measurement of the temperature gradient over a defined geometry, in response to a known power input, allows for a direct calculation of the thermal conductance of the system.

The dimensions of the device are designed to minimize error in the measurement of the thermal conductance. Specifically, the dimensions are designed to localize heat dissipation to within the SiN bridges and to minimize heat loss to radiation. For example, the dimensions of the SiN bridges are designed such that the total thermal conductance through the four bridges is at least 10 times greater than that of the two legs that connect to the membrane PRT. In addition, the resistance of the of the PRT on the membrane is designed to be more than 10 times larger than that of the two legs which extend to the substrate so that the majority of the heat is dissipated within the membrane and that the measured resistance is representative of the PRT on top of the membrane. Moreover, the width of the serpentine PRT is varied to achieve a nearly isothermal profile.

While the devices are designed so that heat predominately conducts through the SiN membrane, we consider heat loss through other mechanisms. Analysis of the thermal resistance provides for a quantitative comparison. First, we note that the devices are operated in a vacuum on the order of 10^{-6} Torr, and thus convective heat losses are negligible, which we have verified in similar devices (see supplementary material). Beyond convective heat losses, the thermal contact resistance ($R_{th,cont}$) and thermal resistance of radiation ($R_{th,rad}$) are considered. Cho et al. [30] report interfacial thermal resistances ranging from 4.8×10^{-9} - 7.5×10^{-9} m^2 K W^{-1} for Al-SiN interfaces at room temperature (which would increase at lower temperatures). Kimling et al. [31] have reported a similar contact resistance of 3.3×10^{-9} m^2 K W^{-1} for Pt/dielectric (SiO_2) interfaces. Assuming this lower value of 3.3×10^{-9} m^2 K W^{-1} would yield a minimum $R_{th,cont}$ of 19 K W^{-1} (given that the area for vertical conduction across the PRT-SiN interface is approximately 170 μm^2). We calculate $R_{th,rad}$ as [32],

$$R_{th,rad} = \frac{1}{h_r A_s}, h_r \equiv \sigma\epsilon(T + T_0)(T^2 + T_0^2) \qquad (1)$$

where ϵ is the material emissivity, σ is the Stefan-Boltzmann constant, T is the device temperature, T_0 is the surrounding temperature, and A_s is the device surface area. In the case of bulk SiN, a common estimation for the emissivity is $\epsilon = 0.6$ [33]. However, Zhang et al. [34] have shown that for freestanding silicon nitride membranes, the value is thickness-dependent, and can be much smaller than the bulk value. van Zwol et al. [35] have likewise shown that the emissivity of freestanding SiN membranes vanishes as the thickness is reduced. However, when coated with thin metal layers, the emissivity can approximately recover to that of the theoretical limit of a thin metal film ($\epsilon = 0.5$) [35]. Therefore, we assume an emissivity of 0.5 and set A_s equal to the surface area covered by the PRT on the membrane ($\sim$170 μm^2) in our estimation of $R_{th,rad}$. By assuming that the radiative coupling is bidirectional (i.e., the effective surface area is doubled), and a temperature rise of a 5 K, we estimate $R_{th,rad}$ as 9.4×10^8 K W^{-1} at 300 K. Due to the large difference in $R_{th,cont}$ and $R_{th,rad}$, the metal film may be approximated as the same as the SiN temperature [36].

The devices were designed with wide bridges to ensure that heat loss due to to radiation is secondary compared to conduction (i.e, $R_{th,rad} > R_{th,cond}$). For example, the thermal resistance due to conduction through the bridges can be calculated as,

$$R_{th,cond} = \frac{L}{4\kappa A_c}, \tag{2}$$

where L is the length of the bridge, A_c is the cross sectional area, and κ is the thermal conductivity. The factor of four arises from the fact that there are four primary bridges through which heat can conduct. As an example, by assuming 10 μm, 7 μm, and 10 nm for the length, width, and thickness of the bridge, and a thermal conductivity of $\sim$ 1 W m^{-1} K^{-1} at 300 K, $R_{th,cond}$ may be approximated as 3.6×10^7 K W^{-1}. We note that this value is more than an order of magnitude smaller than that calculated for $R_{th,Rad}$ (9.4×10^8 K W^{-1}). Moreover, in a regime where the SiN membrane thickness were increased to a point of having an emissivity closer to that of bulk, $R_{th,rad}$ would still be much larger than $R_{th,cond}$ due to the increase in cross sectional area and thermal conductivity.

The layouts of the of the devices were further optimized by finite element modeling (FEM) using commercial software (COMSOL multiphysics 6.1). With an iterative process, we simulate estimated performance parameters (e.g., thermal and electrical resistances), then modify the dimensions of the device in order to achieve the desired design criteria. For example, we modify the width and lengths of the SiN bridges to ensure that thermal conductance through the bridges is at least 10 times greater than that of other pathways, and we design the PRT such that the bulk the of electrical resistance is localized atop the membrane. Fig. 3(a) displays an example temperature profile of a 120 nm thick device in response to a DC current of 2.5 μA applied to the PRT. The induced temperature rise of a cross section, indicated by the dashed line, is shown as a function of time and space in 3(b) and (c), respectively. The spatial temperature distribution in (c) illustrates an approximately isothermal profile within the central membrane and linear gradient along the bridge.

III. Fabrication

Following preliminary modeling, the suspended devices were fabricated through a series of etching and lithographic processes. Nominally 120 nm and 20 nm films of LPCVD SiN were deposited upon (100) silicon wafers, which were subsequently diced into square pieces, 5 mm on a side. Several pieces of the 120 nm and 20 nm films were thinned using an RIE process to produce additional film thicknesses nominally 60 nm and 10 nm thick. An Oxford Instruments Plasmalab 80 Plus was used for the SiN RIE process. The chamber is maintained at a temperature of 20 °C and evacuated to a pressure of 30 mT. We utilize an RF power of 100 W, and gas flow rates of 5 sccm, 5 sccm, and 40 sccm for Ar, O_2, and CF_4, respectively. These conditions provide an etch rate of approximately 3.3 Å/s. The final SiN film thicknesses for the devices are listed in Table I. Measurements were made using the same spectroscopic reflectometer mentioned earlier. Electron beam and optical lithography techniques were used to pattern the serpentine PRTs and contact pads on to each sample. The PRTs were fabricated using a liftoff method with electron-beam-deposited Pt, nominally 10 nm thick. Cr (5 nm) was used as the adhesion layer, which performs better than Ti in fluorine-based etchants. The contact pads were 100 nm thick Au films, which utilized a 10 nm Cr adhesion layer.

TABLE I

Measured Dimensions for Each Device: Membrane Thickness (d), Bridge Length (l_{bridge}), Bridge Width (w_{bridge}), Length of the Legs (Which Connect the Membrane PRT to the Substrate, l_{leg}), Leg Width (w_{leg}), and Width of the Pt Metal Atop the Leg ($w_{leg,Pt}$)

$d_{nominal}$ (nm)	d (nm)	l_{bridge} (μm)	w_{bridge} (μm)	l_{leg} (μm)	$w_{leg,Pt}$ (nm)	w_{leg} (nm)
120	119	10	7	8.39	83	220
60	64	10	7	8.37	111	368
20	18	9.9	6.9	8.37	124	270
10	8.7	10	6.9	8	117	117

After metal deposition, trapezoidal shapes were patterned via electron beam lithography to produce regions defining the outline of the membrane. The trapezoidal regions were developed, leaving exposed regions of SiN film, which were subsequently removed with an RIE process to expose the underlying Si substrate. The devices were then suspended with a silicon etch process by submersing them into 36 wt. % KOH etchant at 60 °C for 60 minutes. Critical point drying (Tousimis Autosamdri-815, Series A) was required for the thinnest devices (10, 20 nm) to prevent membrane collapse. Thicker membranes were successfully released by submersing the etched devices in methanol prior to air drying [37] followed by an O_2 plasma clean to remove any residual solvent. The final device platforms consist of a 20 μm $\times$ 20 μm membrane, four 10 μm $\times$ 7 μm bridges, as well as two thin legs that connect the membrane PRT to the substrate. A scanning electron microscope image of the nominally 20 nm thick device is displayed in Fig. 3(d). The actual dimensions for each device are tabulated in Table I.

IV. Measurement

Following fabrication, the electrical properties of the PRTs were characterized in cryogenic conditions. We utilize a similar measurement setup discussed previously [38], [39], [40], which consists of a Janis CCS-450 cryocooler outfitted for electrical testing. The devices were wire-bonded (WestBond 747677E-79C) into chip carriers (Spectrum Semiconductor Materials CSB02842) housed within the cryocooler. We perform precise "cold wire" measurements by applying a 20 nA alternating current (Keithley 6221) to the PRTs and measuring the voltage drop across each with a lock-in amplifier (Stanford Research Systems SR830). $R(T)$ is calibrated for each PRT by measuring the resistance at temperatures ranging from 10 K - 300 K. An example of the temperature-dependent resistance of the 120 nm membrane PRT is shown in Fig. 4(a). From $R(T)$, we then calculate the temperature coefficient of resistance (TCR), or $\beta(T)$, as

$$\beta(T) = \frac{1}{R(T)}\frac{dR(T)}{dT}. \tag{3}$$

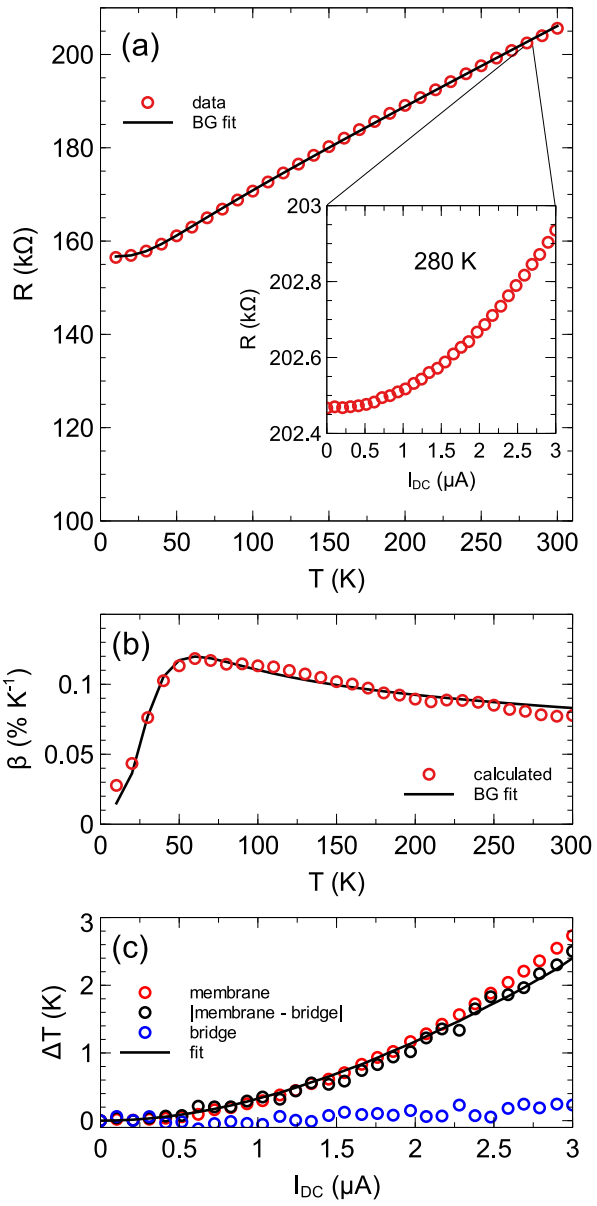

Fig. 4. Example of data collected from a 120 nm thick device. (a) displays the temperature-dependent resistance of the resistor on the membrane. At each temperature, the resistance is then monitored in response to a DC current sweep. The inset of (a) shows an example of the DC current dependent resistance at $T_0 = 280$ K. The data is fit with a Bloch-Grüneisen model to establish a temperature-dependent function for the resistance. The temperature coefficient of resistance, $\beta(T)$ is calculated for both the membrane and bridge resistors (b). (c) displays the corresponding temperature rise of the membrane and bridge resistors, which is subsequently modeled to find the thermal conductivity.

Fig. 4(b) shows the TCR for the PRT in (a). Generally, the TCR of PRTs is on the order 0.003 K^{-1} near room temperature [40], [41], however, the TCR of these devices is lower due to their thinness (nominally 10 nm), which increases the degree of electronic boundary scattering [42], [43]. As small deviations in the measurement can have a large influence on the calculated TCR, we minimize error through sampling (5,000 or more samples per resistance measurement at each temperature). In addition, we apply a Bloch-Grüneisen (BG) fit to the temperature resistance to generate smooth model fits for $R(T)$ and $\beta(T)$ [14], [40]. As an example, the result of the BG fit for the nominally 120 nm thick sample is plotted over $R(T)$ and $\beta(T)$ data in Figs. 4(a) and (b).

To examine the thermal conductance properties of the devices, the PRT resistances were also measured in response to sweeps of DC current, I_{DC}. 5,000 - 10,000 samples of AC sensing current were averaged for each I_{DC} to reduce random noise. I_{DC} varied between 200 nA to 3 μA, depending upon the cryo temperature and SiN thickness to ensure the regulated temperature rise at the membrane remained on the order of several degrees Kelvin. The inset of Fig. 4(a) displays an example sweep of the nominally 120 nm thick sample performed at an ambient temperature of 280 K. It is important to note that for resistance thermometry techniques which employ an AC sensing current combined with a DC heating current, a factor of 3 reduction in the actual temperature rise can occur depending upon the frequency regime. For example, Shi et al. [8] have shown that at low frequencies, there is a nontrivial first harmonic oscillation in the resistance measured by the lock-in amplifier that gives rise to the factor of 3 in the resultant temperature rise. This phenomenon has also been discussed by Dames and Chen [44] in a derivation of the electrical transfer function of the 3ω technique. This factor of 3 reduction in the temperature rise also translates into a factor 3 reduction in the resistance increase measured by the lock in. More explicitly, $\Delta R = \Delta R_{measured}/3$. And thus, a corrected value for the resistance can be obtained as, $(R_{measured} - R_0)/3 + R_0$.

For our measurements, the sensing current frequencies applied to the membrane and bridge resistor were 13.1 Hz and 111.7 Hz, respectively. Frequency sweeps of the sensing currents were performed at several temperatures to confirm that the applied frequencies were in a low-f regime in which the measured lock-in values maintained a wide margin of frequency-independence. Therefore, measured $R(T)$ values were corrected using the aforementioned correction factor. In addition, we verify the resistance obtained from the AC sensing method by ensuring it provides the same result as a purely DC method. An example comparison is provided in the supplementary material.

In the regime of small temperature excursions on the order of a few degrees Kelvin, a linear temperature-dependent resistance may be assumed such that,

$$R(T) = R_0(T)(1 + \beta(T)\Delta T) \tag{4}$$

where $R_0(T)$ is the resistance of the resistor at a given ambient temperature when no DC current is applied and ΔT is the temperature rise induced by Joule heating. By rearranging Eq. 4, the temperature rise may then be expressed as,

$$\Delta T = \frac{1}{\beta(T)}\left(\frac{R(T)}{R_0(T)} - 1\right). \tag{5}$$

Fig. 4(c) displays the temperature rise for both the membrane and bridge PRTs as a function of I_{DC}. By taking the difference in ΔT for the membrane and bridge PRTs, the temperature gradient along the length of the bridge can then be established.

If the device geometry and steady-state temperature rise in response to a given input power are known, the thermal conductivity may be calculated from Fourier's Law,

$$\dot{Q}(T) = -\kappa(T) A_c \nabla T, \tag{6}$$

where $\dot{Q}(T)$ is the heat rate over a cross sectional area A_c, and $\kappa(T)$ is thermal conductivity. As the thermal conduction is one-dimensional along the length the SiN bridge, the temperature difference, ΔT, along the length of the bridge, may be solved for as,

$$\Delta T = \frac{\dot{Q}(T)}{A_c}\frac{L}{\kappa(T)} = \frac{I_{DC}^2 R(T)}{A_c}\frac{L}{\kappa(T)}, \tag{7}$$

where L is the length of the SiN bridge between the PRTs, and the heating is due to Joule heating from the DC current ($I_{DC}^2 R(T)$). We use Eq. 7 to model the temperature rise of each I_{DC} sweep, and treat $\kappa(T)$ as a fitted parameter. As the thermal conductivity is a function of T, we limit the DC heating to only raise the temperature by a few degrees above T_0.

The membrane PRTs are designed to provide an approximately isothermal profile along the span of the membrane. However, the average, measured temperature rise (which we refer to as $\Delta T_{mem,avg}$) is slightly higher than that near the perimeter. We term the temperature rise near the edge of the PRT, adjacent to the SiN bridge, as $\Delta T_{bridge,edge}$. The temperature rise at the thermometer on the bridge nearer the substrate is termed $\Delta T_{bridge,thrm}$ (c.f. Fig. 3(b)). COMSOL simulations are utilized to calculate $\Delta T_{bridge,edge}$, and establish a ratio of $\Delta T_{bridge,edge}/\Delta T_{mem,avg}$. The ratio varies with film thickness, and is found to be 0.86, 0.88, 0.93, and 0.95 for the nominally 120, 60, 20, and 10 nm membranes, respectively, and remains relatively constant as a function of temperature. The measured temperature gradients are scaled to obtain $\Delta T_{mem,edge}$, and the temperature gradient along the span of the bridge, ΔT, is calculated as $\Delta T_{bridge,edge}$ - $\Delta T_{bridge,thrm}$

An additional consideration in the measured temperature rise is the heat loss from the PRT along the legs that connect it to the substrate. The rate of heat loss along each leg $\dot{Q}_{leg}$ is subtracted from the total $\dot{Q}(T)$ generated from Joule heating. The thermal conductivity of the SiN film is initially obtained without considering heat loss along the two legs. Then, from the initially obtained thermal conductivity, we consider $\dot{Q}_{leg} = G_{leg}\Delta T_{leg}$, where $G_{leg} = G_{leg,metal} + G_{leg,SiN}$ and $\Delta T_{leg} = \Delta T_{leg,edge}$. $\Delta T_{leg,edge}$ is obtained from COMSOL simulations similar to those used to determine the ratio of the average measured temperature rise and that of the bridge edge. The thermal conductivity of the metal leg is calculated with the Wiedemann-Franz law (WFL) resulting in values of 8.2 W m^{-1} K^{-1} - 11 W m^{-1} K^{-1} at room temperature, depending upon the sample (see supplementary material). These values are subsequently used to obtain $G_{leg,metal}$. We then iteratively obtain the thermal conductivity of SiN until the obtained value converges within a tolerance of 1%. We note that assumption of the WFL serves as a lower bound to the thermal conductivity of the Pt as prior works have demonstrated that phonon contributions can yield a higher apparent value in thin Pt films [48], [49]. For example, Zhang et al. [49] report a thermal conductivity of 29.5 W m^{-1} K^{-1} for a 28-nm-thick evaporated Pt film, nearly a factor of two higher than that expected from the WFL. As our PRTs employ thinner Pt, a lower thermal conductivity is expected. However, in consideration of an increased Pt thermal conductivity due to an enhanced phonon contribution, we consider an upper bound of twice the value calculated from the WFL. The shaded regions in Fig. 5 outline upper and lower bounds for the resultant thermal conductivity of the SiN membranes from this range of Pt thermal conductivity values. The influence is most pronounced on the thinnest membranes. For example, a factor of two increase in Pt thermal conductivity would result in a 13% reduction in the thermal conductivity of the thinnest SiN membrane at (room temperature), with subsequently smaller impacts as the membrane thickness is increased.

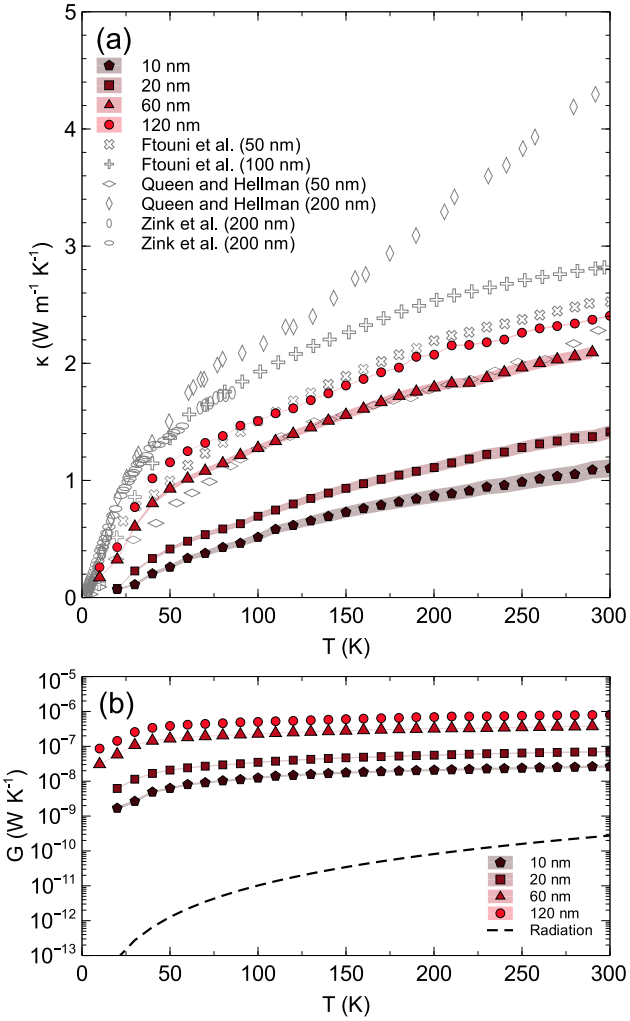

Fig. 5. Thermal conductivity (a) and thermal conductance (b) obtained from analysis of the temperature rise measurements. For comparison, the thermal conductivity of several other LPCVD SiN membranes (References [45], [46], and [47]) is plotted in (a). The dashed line in (b) displays the estimated thermal conductance due to radiation based upon Eq.1.

V. Results and Discussion

The thermal conductivity for each device is displayed in Fig. 5(a). In all cases, the temperature-dependence of the

thermal conductivity follows an expected glass-like trend [50], which increases as a function of temperature. Additionally, a thickness-dependent trend is observed. At room temperature, the thermal conductivity ranges from 1.1 W m^{-1} K^{-1} - 2.4 W m^{-1} K^{-1} depending upon the thickness. To contextualize these results, we compare the thermal conductivity to other measurements performed upon SiN membrane structures reported in the literature. Ftouni et al. [45] used a 3ω-Völklein method to demonstrate that the thermal conductivity of SiN membranes is insensitive to film stress for membranes 50 nm and 100 nm thick. Queen and Hellman [46] and Zink et al. [47] used microcalorimeter type devices to measure the thermal conductivity of thin, continuous membranes. Generally, we find the thermal conductivity of the membranes in this study to be consistent with those of prior works. For example, the temperature-dependence of the nominally 60 nm film is comparable to that of the 50 nm film measured by Queen and Hellman, and slightly lower than the 50 nm film reported by Ftouni et al. The thinner films (20 nm, 10 nm) demonstrate a significantly lower thermal conductivity than the thicker films, and are among the lowest reported for films prepared by an LPCVD process [51]. Despite SiN being amorphous, size effects have been observed and are generally accredited to a reduction in the thermal carrier mean free path [45], [46].

Reducing membrane thermal conductivity is desirable for devices that rely upon thermal isolation. For example, calorimeter and bolometer performance is fundamentally limited by the conductive coupling of the device with its surrounding [52]. Thus, suspended devices with minimized thermal conductances are ideal. For reference, we calculate the temperature-dependent thermal conductance, $G(T)$, of the devices in Fig. 5(b) using the thermal conductivity in (a). $G(T)$ is calculated by inverting Eq. 2. We note that because the coefficient of thermal expansion for silicon nitride is on the order of 10^{-6} K^{-1} (see references [53] and [54]), A_c is assumed to be independent of temperature over the measured range. Despite having wide bridges, the devices maintain low thermal conductances, ranging from 2.7×10^{-8} W K^{-1} to 8.0×10^{-7} W K^{-1} at 300 K, depending on the membrane thickness. If the bridge widths are reduced, to a value closer to 100 nm, such as in Fig. 2, the thermal conductance could be decreased by orders of magnitude. For example, a device with bridges 10 μm in length, 100 nm wide, and 10 nm thick could be expected to provide a thermal conductance of approximately 4.4×10^{-10} W K^{-1}. If the surface of the membrane were coated with an absorbent film [55], the conductance due to radiation could become the dominant source of thermal transport, providing an ideal operating condition for bolometry [38], [52], [56].

VI. Summary

In summary, we report on the development and thermal measurement of suspended SiN membrane devices with thickness ranging from over 100 nm to less than 10 nm. Films are produced with an LPCVD process providing a low-tensile intrinsic stress (< 300 MPa for all thicknesses). A top-side etch method enables fabrication of suspended membranes with tethers tens of nanometers thick and tens of nanometers wide. For thermal characterization, we design devices with wide tethers to enhance measurement sensitivity to conduction through the tethers. We fabricate devices with thicknesses ranging from 119 nm to less than 10 nm, and measure the thermal conductivity and thermal conductance from 10 K to 300 K. We find thermal conductivities ranging from 1.1 W m^{-1} K^{-1} to 2.4 W m^{-1} K^{-1} near room temperature. The thermal conductivity of the thinnest films is among the lowest reported for LPCVD SiN. If similar devices are created with tether thicknesses and widths on the order of tens of nanometers, thermal conductances (due to conduction) on the order of 10^{-10} W K^{-1} may be expected. This has positive implications for bolometer and calorimeter devices, and provides a path toward achieving devices with ultra low thermal conductance that may fit within an envelope relevant to commercial standards.

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